instruction and including an address for the at least one instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

reading the instruction or data in accordance with the address for the instruction or the address for the data with the first unit;

storing the instruction or the data in a buffer; and

executing the stored instruction with a second unit.

2. (Amended) The method of claim 1, wherein the first unit includes a pseudo instruction detection unit connected in parallel with the buffer, wherein the step of detecting the pseudo instruction includes supplying the program read from the memory to the pseudo instruction detection unit in parallel with the buffer.

3. (Amended) The method of claim 1, wherein the buffer includes first and second buffers connected in parallel with the memory, and the method further comprising a step of storing the instruction and data read from the memory in the first buffer and storing the instruction or data included in the detected pseudo instruction in the second buffer.

4. (Amended) The method of claim 3, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the first buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with the at least one instruction address or data address with the first unit after the transfer of the at least one instruction to the first buffer has been identified.

5. (Amended) The method of claim 4, further comprising the step of identifying that the corresponding instruction or data is stored in the second buffer in accordance with the at least one instruction address or data address when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction or data is not stored in the second buffer.

6. (Amended) The method of claim 1, further comprising the steps of:

identifying that at least one instruction following the pseudo instruction has been transferred to the buffer with the first unit when the pseudo instruction is detected; and

prefetching the instruction or data from the memory in accordance with at least one instruction address or data address with the first unit after the transfer of at least one instruction to the buffer has been identified.

7. (Amended) The method of claim 6, further comprising the step of identifying that the corresponding instruction or data is stored in the buffer in accordance with the at least one instruction address or data address with the first unit

when the pseudo instruction is detected, wherein the prefetch step is executed when the corresponding instruction or data is not stored in the buffer.

8. (Twice Amended) A microcontroller, comprising:

a buffer, connected to a memory, for storing instructions and data of a program read from the memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the at least one instruction or an address for data;

a first unit including,

a pseudo instruction detection unit, connected to the memory, for detecting the pseudo instruction included in the program read from the memory; and

an address control unit, connected to the external memory and the pseudo instruction detection unit, for reading the instruction or data in accordance with the address for the instruction or the address for the data and storing the instruction or the data in the buffer; and

a second unit connected to the buffer, for executing the instruction stored in the buffer.

9. (Amended) The microcontroller of claim 8, wherein the buffer includes first and second buffers connected in parallel with the memory, wherein the first buffer stores the instruction and data read from the memory, and the second buffer stores the instruction or data included in the detected pseudo instruction.

14. (Twice Amended) A device for detecting a pseudo instruction preset before a specific instruction, wherein the pseudo instruction includes an opcode and an operand, and wherein the device is independent of an instruction execution unit for executing the specific instruction, the device comprising:

a detection circuit, connected to a data line, for receiving the pseudo instruction transferred on the data line and detecting the opcode included in the pseudo instruction; and

a detection timing circuit, connected to the detection circuit, for calculating instruction length or the number of operands of the pseudo instruction from the opcode and determining the transfer period of the opcode based on the instruction length or the number of operands, wherein the detection timing circuit supplies a signal for invalidating the opcode detection operation during an operand transfer period.

16. (Twice Amended) A microcontroller connected to a memory which stores instructions and data, the microcontroller comprising:

an instruction execution unit for reading instructions and data from the memory and processing the read instructions; and

a prefetch circuit unit that receives instructions and data read from the memory in response to a fetch signal, and detects pseudo instructions included in the instructions and data, wherein a pseudo instruction precedes a branch instruction and indicates the existence of the branch instruction, and wherein the prefetch circuit is independent of the instruction execution unit;

wherein the prefetch circuit unit includes,

a prefetch buffer connected between the instruction execution unit and the memory for temporarily storing instructions and data being transferred from the memory to the instruction execution unit,

a bus interconnecting the prefetch buffer and the memory,

a pseudo instruction detection unit connected to the bus for detecting pseudo instructions among the instructions and data being transferred from the memory to the prefetch buffer,

a holding circuit, connected to the bus and to the pseudo instruction detection unit, for storing operands of the pseudo instruction,

a pseudo instruction buffer for temporarily storing instructions and data fetched from a location in the memory which is pointed to by the branch instruction following the pseudo instruction,

an address control unit for generating the fetch signal and for generating a memory address which points to the address of a next word to be read from the memory, and wherein when the pseudo instruction detection unit detects a pseudo instruction, the instructions and data pointed to by the pseudo instruction are fetched from the memory by the address control unit and stored in the pseudo instruction buffer so that when the branch instruction following the pseudo instruction is processed by the instruction execution unit, if the branch is taken, the instructions and data pointed to by the branch instruction have been prefetched and stored in the pseudo instruction buffer.

Please add new claims 24-34, as follows:

24. (New) The method of claim 1, wherein the pseudo instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

25. (New) The method of claim 1, further comprising executing a no-operation (NOP) instruction in accordance with a detection of the pseudo instruction.

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26. (New) The method of claim 1, further comprising counting the address for the at least one instruction or the address for data so that the second unit skips the pseudo instruction.

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27. (New) The microcontroller of claim 8, wherein the pseudo instruction is one of an unconditional branch instruction, a conditional branch instruction, a CALL instruction, and a data calling instruction.

28 (New) The microcontroller of claim 8, wherein the second unit executes a no-operation (NOP) operation in accordance with a detection of the pseudo instruction.

29. (New) the microcontroller of claim 8, wherein the second unit includes an address counter for counting the address for the at least one instruction or the address for data so that the second unit skips the pseudo instruction.

30. (New) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

prefetching the instruction or data in accordance with the detection of the pseudo instruction with the first unit; and

executing a no-operation (NOP) operation with a second unit in accordance with the detection of the pseudo instruction.

31. (New) A method for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the method comprising the steps of:

reading the program from the memory;

detecting the pseudo instruction with a first unit;

prefetching the instruction or data in accordance with the detection of the pseudo instruction with the first unit; and

counting the address for the at least one instruction or the address for data so that a second unit, which is independent of the first unit, skips the pseudo instruction and executes the prefetched instruction.

32. (New) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data in accordance with the detection of the pseudo instruction; and

a second unit for executing a no-operation (NOP) operation in accordance with the detection of the pseudo instruction.

33. (New) An apparatus for prefetching instructions and data of a program stored in a memory, wherein the program includes a pseudo instruction and at least one instruction, the pseudo instruction being arranged before the at least one instruction and including an address for the instruction or an address for data, the apparatus comprising:

a first unit for reading the program from the memory and detecting the pseudo instruction, wherein the first unit prefetches the instruction or data in accordance with the detection of the pseudo instruction; and